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A STUDY ON PROCESS LIMITATIONS AND SCOPES OF MICRO-MANUFACTURING TECHNIQUES FOR THE FABRICATION OF MEMS TORSIONAL ACTUATORS

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ABSTRACT

A theoretical study on the various micro fabrication techniques such as surface micromaching, Silicon-On-Insulator (SOI), polyMUMPS, and identifying the process limitations and suggesting new scopes in the microfabrication process sequence for the development of MEMS devices with better performance. A multi-layer, multi-step lithography process is used in fabrication of micro actuators in silicon as base materials and oxide layers and metal layers combination. Selective deposition of metal on microstructures using poly silicon multi user MEMS process (polyMUMPS). The deposited metal layer thickness invariably induces tensile or compressive residual stress which will affect the operating characteristics the device. The fabrication sequences such as deposition, etching, annealing at different temperature level significantly affect the mechanical properties of the torsional type switching device. The deposited metal increases the stiffness and the effective mass of the laminated structure. The residual stress increases or decreases the net stiffness if it is a tensile or compressive type respectively. The *process-induced* residual stresses present in the planer structures of the micro-switch should be reduced for its effective and improved performance.

Key words: *Microfabrication, Surface Micromachining, PolyMUMPS, SOI, Process-induced residual stress, Thin plate electrodes and Film Thickness*

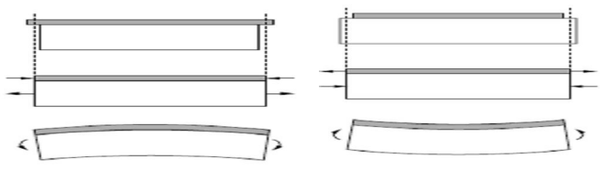
1. Introduction

The deposited thin film on the substrate layer, which initially shrinks relative to the substrate. Generally, the base substrate layer dimensions change with little shrinkage in the plane while the deposited thin film dimensions reduce remarkably. For structural compatibility it is required that the both the thin film and substrate have the same length. Therefore, the film is constrained and stretches, while the substrate accordingly contracts.

If tensile forces are developed in the deposited thin film then they are balanced by the compressive forces in the substrate. The force balance is still not in mechanical equilibrium because of the uncompensated end moments. The mechanical equilibrium is reached when the compressive and tensile forces and corresponding bending moments should disappear from film/substrate cross section.

If the structure is free to move, it will elastically bend to counteract the unbalanced moments. The deposited thin films containing internal tensile stresses try to bend the substrate concave upward. Similarly, compressive stresses from films tend to initially expand relative to the substrate; bend the substrate convex outward.

The extrinsic stresses are caused by temperature gradients. It is generally uniform through the depth. Thermal-mismatch stress is the more common source of residual stress. It specially arises in structures with inhomogeneous coefficient thermal expansion (CTE), subjected to uniform temperature change



(a) (b)

Figure 2.2: Sequence of Events Leading to (a) Residual Tensile Stress in Film; (b) Residual Compressive Stress in Film

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Microelectromechanical systems (MEMS) torsional micro-actuators are electromechanical switches in micron scale range which are used to tilt the optical beams in scanning/ switching applications. Torsional thin plate top electrode is driven in lilting motion by electrostatic attraction force towards left and right half bottom electrodes alternatively.

A multi-layer, multi-step lithography process is used in fabrication of micro actuators in silicon as base materials and oxide layers and metal layers combination. Selective deposition of metal on microstructures using poly silicon multi user MEMS process (polyMUMPS). The deposited metal layer invariably induces tensile or compressive residual stress which will affect / influences the operating characteristics the device.

The fabrication sequences such as deposition, etching, annealing at different temperature level significantly affect the mechanical properties of the switching device. The deposited metal increases the stiffness and the effective mass of the laminated structure. The residual stress increases or decreases the net stiffness if it is a tensile or compressive type respectively.

The process-induced residual stresses present in the planer structures of the micro-switch should be eliminated for its effective and improved performance. The mechanical parameters could be tailored to suit the need of the switching device performance. There are numerous factors which alter the resonant frequency of the fabricated device such as the metal layer deposited on top of the torsional plate electrode and the residual stresses. For this we carried out a detailed theoretical study on the various micro fabrication techniques such as surface micromaching, Silicon-On-Insulator (SOI), polyMUMPS, SUMMiT.

Residual stresses in thin deposited films always pose a big challenge during the design and fabrication of MEMS devices. The majority of thin film deposition techniques produce residual stresses in the deposited films

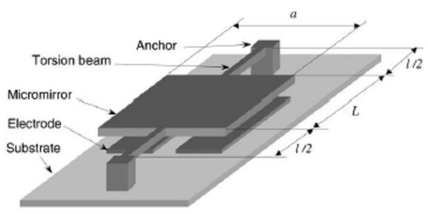


Fig.1 MEMS Torsional Micro Actuator

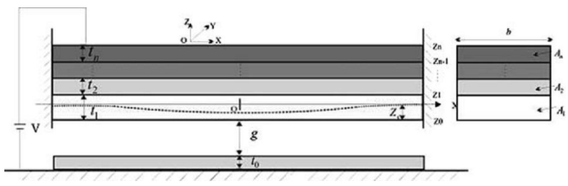


Fig. 2 Multi-layered Structure Cross Sectional View

2. Micro Fabrication Process Types

2.1 PolyMUMPS

MEMSCAP provides three standard processes as part of the MUMPs program. The Multi-User MEMS Processes, known as MUMPs, is a program that offers cost-effective MEMS fabrication solution to industry, research labs in universities, and government research centers worldwide. PolyMUMPs, a three-layer polysilicon surface micromachining process. MetalMUMPs, an electroplated nickel process; and a silicon-on insulator micromachining process known as SOIMUMPs.

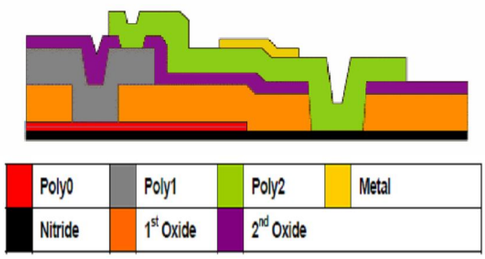


Fig. 3 All 7 Layers of the PolyMUMPs Process in Cross Sectional View

PolyMUMPs processes have the general features of a standard surface micromachining process: (1) polysilicon is deposited as the structural material, (2) deposited oxide phospho silicate glass (PSG) is deposited as the sacrificial layer, and silicon nitride (Si3N4) is used as electrical isolation layer between the polysilicon and the substrate.These processes are different from the generalized surface micromachining processes in that they are designed to be as liberal as possible, and to be capable of supporting many different designs on a single silicon wafer. The thicknesses of the structural and sacrificial layers are selected to meet the needs of most users, and the device layout design rules are selected in conservative manner to ensure the maximum yield possible.

This data on stacked polysilicon devices, using direct stress-strain measurements is preliminary, as it is based on devices made over a sampling of PolyMUMPs runs [3].

Table 1: Thickness Vs Residual stresses of Multilayers [3]

Film	Thickness (A°)			Residual stress (Mpa)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Nitride	5300	6000	6700	0	90	180
Poly0	4700	5000	5300	0	-25	-50
Oxide1	17500	20000	22500	N/A		
Poly1	18500	20000	21500	0	-10	-20
Oxide2	6700	7500	8300	N/A		
Poly2	14000	15000	16000	0	-10	-20
Metal	4600	5200	5800	0	50	100

2.2 Summit

SUMMiT V (Sandia Ultra-planar Multi-level MEMS Technology V) is a 1.0 µm, 5-level, surface micromachining (SMM) technology offers four structural layers of polysilicon fabricated above a thin highly doped polysilicon electrical interconnect and ground plane layer. Sacrificial oxide layer is deposited between each polysilicon level in sandwiched manner. The thin sacrificial film defines the amount of mechanical motion. By using a chemical mechanical polishing (CMP) process, the oxide layer directly beneath the upper two levels of structural polysilicon are planarized. This step alleviates several photolithographic and film etching steps. It also removes the design constraints that would otherwise be imposed by the underlying topography. An optional patterned metal layer can be deposited to the top polysilicon layer for electrical interface connections.

2.3 MUMPS and SOI technologies

The proposed model in the literature which will be useful in understanding the performance of torsional micromirrors subjected to large tilting angles. The scanning micromirrors were analysed for static angles and natural frequency considering two different types of microfabrication technologies. Different designs were considered and analyzed based on MUMPS and SOI technologies. The gap between the electrodes in MUMPS becomes the limiting factor in designing the maximum tilt angle

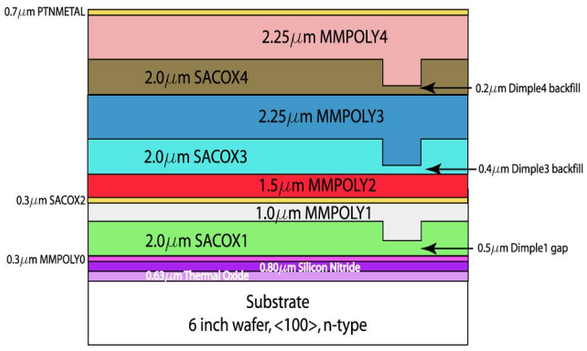


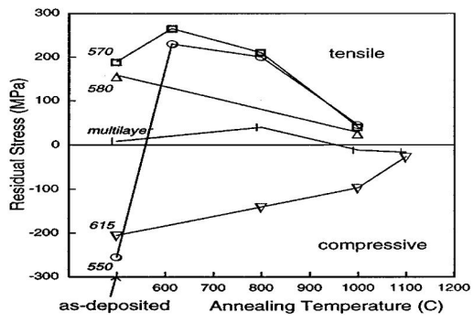
Fig. 4 SUMMiT V™ Structural and Sacrificial Layers

2.5 The multipoly and epipoly processes

A process for fabricating polysilicon films with near-zero stress, near-zero stress gradients, with a maximum temperature is 615° C in this process. Though these films are deposited at relatively low temperatures, the total stresses remain unaffected by annealing process done at high-temperature. Deposition of alternate tensile fine-grained and compressive columnar layers of polysilicon, which are deposited at growth temperatures of 570° and 615° C, respectively in this process. The fabrication of a multi-layer low-stress, low-stress gradient MultiPoly film was demonstrated.
In addition, alternating multilayers of polysilicon and SiO2 have been proposed as a low-stress film and a low-stress bilayer composed of compressive polysilicon deposited at 600° C and 100-mTorr silane, and tensile polysilicon deposited at 600° C and 200-mTorr silane has been reported. The substrates that include integrated circuits can be adversely affected by large thermal budgets.

The use of multilayers of polysilicon, deposited at varying temperatures at or below 615° C, which individually possess residual stresses but of opposite sign, and when combined into multilayer films display overall near-zero stresses and near-zero stress gradients. An apparent disadvantage of the MultiPoly process is that the deposition rates are slow compared to the epipoly process.

The Multi-Poly process also has the capability of “fine tuning” stresses and stress gradients within films through the deposition of additional very thin polysilicon layers if the as-deposited properties are not to specification



3. Role of Various Parameters in Controlling the Residual Stress Level

3.1. Process parameters

The development of microelectronics has adopted the merits brought forth by silicon nitride Si3N4, i.e., passivation layer, barrier against the diffusion of impurity ions or oxidation mask.1, 2. These films are generaly obtained by chemical vapor deposition CVD. from dichlorosilane SiH2Cl2 and ammonia NH3 with an excellent uniformity of film thickness and composition.

Stress reduction can be achieved by decreasing the NH3 /SiH2Cl2 gaseous ratio and by depositing silicon-rich silicon nitride SiNx but deviations to stoichiometry are difficult to achieve and high non uniformity of thickness and composition are induced by this way.

Low stress silicon nitride Si3N4 films were obtained and the most relevant parameters were found as decreasing order of importance, the temperature and the total pressure. By changing the NH3 /SiH4 gaseous ratio, varied SiNx films, i.e., silicon-rich silicon nitride and nitrogen-doped silicon and important stress variations from compressive to tensile values were witnessed.

From all the above results, optimal conditions were pointed out in order to deposit low stress silicon-rich Silicon nitride films. They have been applied for the realization of SiO2 /SiNx membranes for different microelectromechanical devices.

3.2. Film thickness

Generally, a thicker deposited film tends to result in a higher induced residual stress. The effect of the film thickness on the residual stress of the sputtered Cr/Au film was discussed. The largest stress reduction occurs when the Au thickness is reduced from 100 nm (603 MPa) to 70 nm (441 MPa) when the Cr thickness is at 10 nm. When the Cr thickness is decreased to 5 nm with the Au thickness at 70 nm, the film stress further reduces to 403 MPa. However, when the Au thickness is further lowered to 50 nm with the Cr thickness at 5 nm, no further stress reduction can be observed [8].

4. Conclusion

There is a considerable difference in the dimensions of structures fabricated in the bulk and surface micro-machining technology. The vertical dimensions of bulk micro-machined structures are measured by the thickness of the device layer of the SOI wafer used. The surface micro-machined mirrors fabricated from the practical thickness that can be deposited. In the lateral dimensions also the similar differences can be observed. The small dimensions with surface micro-machining technology can result in increased process problems. These are unwanted sticking, bending, and leading to device failure. The large dimensions with bulk micromachining technology will result in low resonant frequencies and large actuation voltage.

A common issue facing both bulk and surface micro-machining technologies is variations in fabrication. These variations arise in both vertical and lateral dimensions. They are resulting from fabrication process, including photolithography, etching, depositing. The fabrication process variation will lead to micro-mirrors being out of specifications of its operating characteristics. Both the dimensions of torsion beams and the thickness of deposited thin-film mirror plates vary across the whole wafer. This variation leads to different performances which are not intended. This is particularly critical for the application of micro-mirror arrays, where the high performance uniformity is required.

As discussed above, there are merits and demerits for all the fabrication technologies. Due to the diversity of applications and requirements for torsion micro-mirrors, different fabrication processes need to be developed to meet the requirements of specific applications. The options come out from the application under development, the mirror geometries in concept and the available micro fabrication equipment.

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