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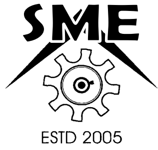

A COMPUTATIONAL MODEL TO PREDICT MATERIAL REMOVAL DEPTH IN WIRE-EDM OF SILICON WAFERS SLICING

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ABSTRACT

Wire-electrical discharge machining (wire-EDM) has the potential to manufacture ultra-thin silicon wafers, significantly enhancing the efficiency of solar photovoltaic cells. However, the fabrication of ultra-thin silicon (Si) wafers through wire-EDM is constrained by its inherently lower material removal rate. This limitation could reduce the throughput rate of solar cell production. Selecting the optimal processing parameters is the key to producing wafers with the maximum material removal rate. The traditional experimental-based optimization is time-consuming and complex. To address this, a computational model of the wire-EDM process is developed. This model aims to predict the material removal depth and identify the best process parameters. The approach involves solving the heat diffusion equation, considering the heating caused by the surface heat flux. The finite element method solves the model equations and evaluates material removal depth by analyzing the simulated temperature profiles. The simulation results indicate that the open voltage significantly influences the material removal depth, compared to pulse on-time. According to the computational model, the calculated material removal depth is 2.5µm when using 74 V and 0.5 µs pulse on time. The study emphasizes the importance of using computational modelling to understand the effect of open voltage and pulse-on time on material removal depth during the wire-EDM process, as it provides valuable insights without experiments. By identifying the material removal depth, this research enhances the efficiency of producing ultra-thin silicon wafers for solar cell manufacturing.

Keywords: *Wire-electrical discharge machining; solar photovoltaic cells; computational modelling; heat diffusion equation; finite element method*

1. Introduction

In recent years, the growing energy demand has led to a significant interest in solar power generation using photovoltaic (PV) cells. To improve the efficiency of solar cells, there is a need to minimize the thickness of silicon (Si) wafers. Currently, used slicing methods can produce wafers with a thickness of 200 µm, but wire-electrical discharge machining (wire-EDM) can slice wafers as thin as 130 µm [1]. While wire-EDM offers the advantage of producing thinner wafers, it also has certain limitations. The material removal process in wire-EDM involves a combination of melting and evaporation, which can generate craters on the work surface [2]. Computational modelling studies have been explored to predict material removal depth, as the traditional approach of conducting numerous experiments to understand the effects of each process parameter is both time-consuming and costly. The computational model currently provides a promising solution for efficient analysis of the influence of process parameters on material removal depth.

In the existing literature, several researchers have attempted to model the material removal depth in wire-EDM using different tools. For instance, Guo et al. [3] utilized the DFULX subroutine in ABAQUS to resolve the singularity issue of Gaussian heat flux. They evaluated the discharge crater with time using temperature profiles. Notably, it is essential to mention that the model described above was developed for die-sinking EDM, and more work must be done on predicting material removal depth specifically for wire-EDM slicing. With the increasing interest in solar power and the drive for more efficient solar cells, the need to produce thinner Si wafers has become crucial. Wire-EDM offers a promising method for achieving this, but its limitations necessitate using computational modelling to optimize process parameters efficiently.

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This research introduces a 2D transient computational model to predict material removal depth in the wire-electrical discharge machining (wire-EDM) context. The governing equation is solved using the finite element method, in the Abaqus™ software. Furthermore, the model serves as a means to explore the specific impacts of open voltage (OV) and pulse on time (T_{on}) on material removal depth. This analysis of the crucial process parameters contributes to an enhanced comprehension of the wire-EDM process. The understanding holds particular significance for using wire-EDM in producing thin silicon wafers tailored for solar cell applications.

2. Modeling Approach

This investigation establishes a specialized 2D axisymmetric model to address the wire-EDM slicing process specifically and anticipate temperature distribution. The rationale underlying this model is substantiated by the observation that the heat diffusion span during an individual pulse is generally small, typically spanning a few micrometres. This magnitude is notably smaller than the workpiece's thickness. Moreover, the pulse on-time adopted in this study falls within the range of 0.3 to 0.5 µs, akin to the discharge duration [1]. Hence, assuming that a single spark occurs during each pulse is reasonable.

Figure 1 illustrates the schematic diagram of this study's utilized 2D axisymmetric model. In the course of the machining process, discharges are anticipated to occur randomly across the surface of the workpiece, particularly in proximity to the wire. The model assumes discharges between the wire and the workpiece to address this scenario. This results in the generation of heat, which leads to an increase in temperature. Further, the energy from the plasma generated during discharges is mostly dissipated as heat within the workpiece, with any remaining energy absorbed by the dielectric. It's important to note that the model's scope is delimited to examining discharge-induced alterations in temperature, excluding other factors such as radiation and wire vibration.

The heating of the workpiece is modelled using the heat diffusion equation given by [4]:

$$k\left(\frac{\partial^2 T}{\partial r^2} + \frac{1}{r}\frac{\partial T}{\partial r} + \frac{\partial^2 T}{\partial z^2}\right) = \rho C \frac{\partial T}{\partial t} + Q_s \quad (1)$$

Equation 1 is solved by considering the surface heat flux resulting from plasma (Q(r)). The regions where the dielectric contacts the workpiece are treated as convective boundaries, while all other surfaces are treated as adiabatic boundaries.

In this equation: ρ represents the density of silicon (measured in kg/m³), k stands for the thermal conductivity of silicon (measured in W/m·K), T represents the temperature (measured in Kelvin), x and y are the coordinate axes, C denotes the specific heat capacity of silicon (measured in J/kg·K).

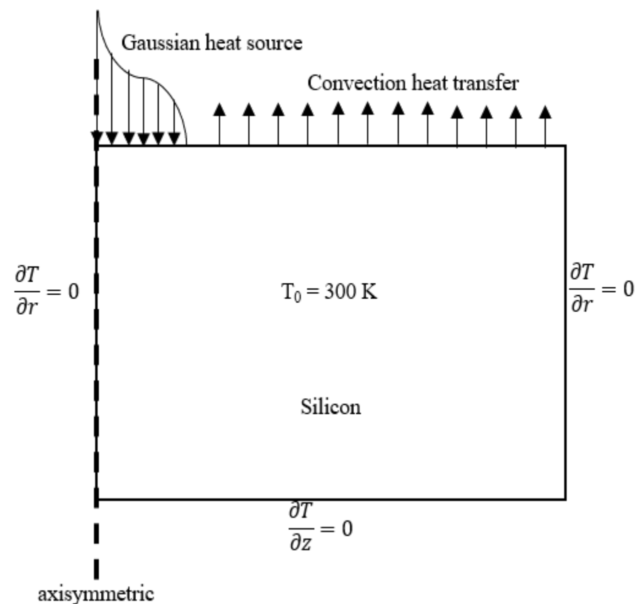

Fig. 1 Model dimension with boundary conditions

The plasma heat source *Q(r)* is given by [5]:

$$Q(r) = \frac{4.45 \times F \times V \times I}{\pi \times R^2} \quad (2)$$

The equation involves various parameters: I denote the discharge current measured in amperes (A). V stands for the discharge voltage in volts (V). R signifies the radius of the plasma channel [6]. F represents the fraction of heat input to the anode surface, assumed to be 18% [7].

$$R = 2040 \times I^{0.43} \times T_{on}^{0.44} \quad (3)$$

For solving the governing equation in Abaqus™, a 4-node linear heat transfer quadrilateral element (DC2D4), typically employed for heat transfer simulations, is chosen. Notably, specific heat, coefficient of thermal expansion, and thermal conductivity are taken to vary with temperature.

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3. Results and discussion

3.1 Temperature profile

Figure 2 displays the temperature distribution obtained with the computational domain. The temperature data is represented by the legend on the left-hand side. Notably, substantial heating is observed exclusively within a narrow vicinity near the discharge zone, spanning micrometres. The simulated temperatures reach extremely high values, particularly within the super-heated zone (nearing 8000 K), owing to the model's omission of material removal caused by evaporation [7]. Material removal can be considered by deleting the elements above silicon's normal boiling temperature (3500~K).

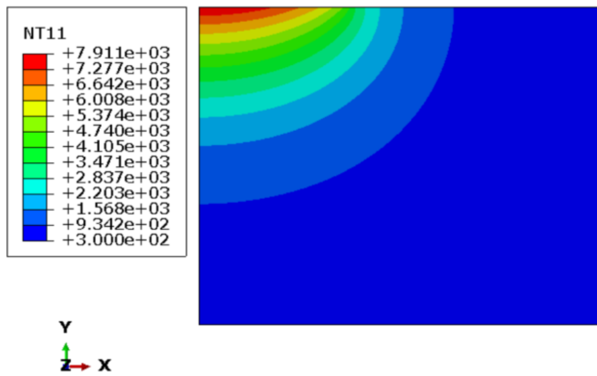

Fig. 2 Temperature contours at OV: 74 V, T_{on}: 0.3 µs

Figure 3 shows the surface temperature at the top left corner of the model at two different processing conditions. Due to a shorter pulse on-time, temperature gradients are very steep. The surface temperature demonstrates a swift decline until it reaches the melting point, followed by a gradual decrease beyond that point.

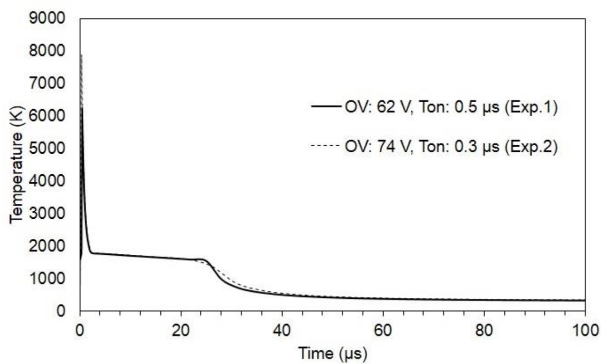

Fig. 3 Variation in surface temperature with time for two processing conditions

Figures 4 and 5 depict the temperature variation along the depth, starting from the top left corner, for two distinct parameter sets. These plots show that the temperature decrease is more pronounced in the Figure 5 set when compared to Figure 4. This discrepancy arises due to the dissimilarity in pulse on time: 0.5 µs in the first set and 0.3 µs in the second. The shorter pulse on time prevents lateral heat diffusion in the wafer, thereby reducing the temperature gradient. Silicon's normal boiling point is approximately 3500 K, a theoretical reference for kerf loss measurement. The melting point of silicon is 1688 K, and its recrystallization temperature is 750 K, which is employed for calculating heat affected zone.

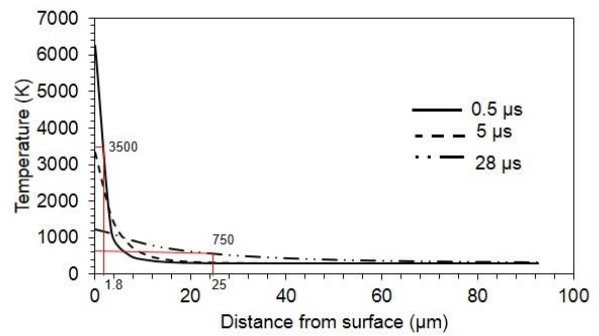

Fig. 4 Variation in temperature with distance at different times for 62V and 0.5 µs

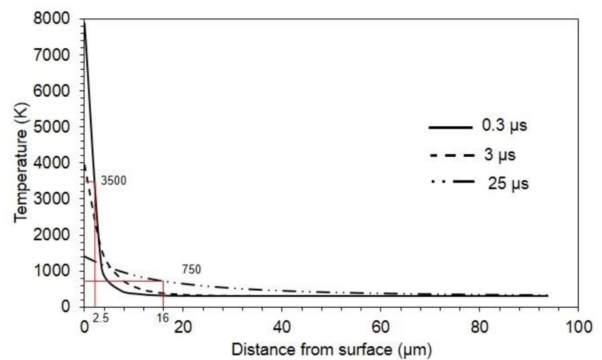

Fig. 5 Variation in temperature with distance at different times for 74V and 0.3 µs

The assumption is that material exceeding 3500 K is directly vaporized, while material within the 1688 K to 3500 K undergoes melting and subsequent re-solidification across the surface. Additionally, material ranging in temperature from 750 K to 1688 K is categorized as the heat-affected zone (HAZ). Consequently, material falling within the 3500 K to 750 K temperature range is designated as the white layer

zone. Based on the information in Figures 4 and 5, the computed material removal depths are determined to be 1.8 μm and 2.5 μm for the first and second sets of process parameters, respectively. The Crater profile generated at the end of the pulse duration for 74V and 0.3 μs is shown in Fig. 6.

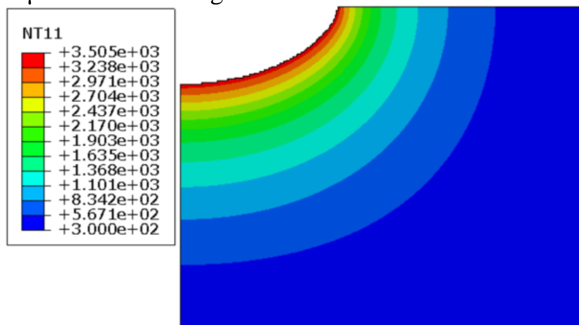

Fig. 6 Crater profile at 74V and 0.3 μs

3.2. Effect of OV and T_{on} on Material Removal Depth

The chosen process parameters predominantly influence the energy generated during the machining process. Specifically, the Open Voltage (OV) and pulse on-time (T_{on}) directly impact the discharge energy. Hence, examining how OV and Ton affect the material removal depth becomes crucial. Figure 7 displays the relationship between material removal depth and pulse on-time for three distinct OV values. Notably, an increase in pulse on time leads to a corresponding rise in material removal depth across all OV values. However, the extent of this increase in material removal depth varies based on the specific OV value. Particularly noteworthy is the observation that the highest growth in material removal depth occurs at an elevated OV of 74 V. Conversely, at a lower voltage of 62 V, the rise in material removal depth is relatively modest.

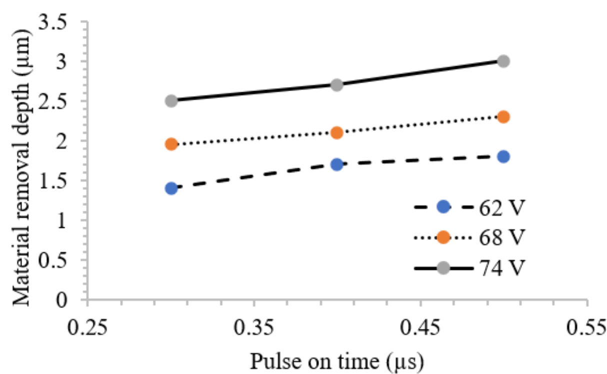

Fig. 7 Variation in material removal depth with a pulse on time at different OV

Likewise, the variation in material removal depth, presented as a function of Open Voltage (OV) for different T_{on} values, is illustrated in Figure 8. In this scenario, the patterns of material removal depth about OV appear consistent across all T_{on} values. Notably, when T_{on} is set at a lower weight (0.3 μs), an escalation in OV is accompanied by an observable rise in material removal depth. This outcome is intuitively expected, as heightened OV increases thermal effects due to the more incredible discharge energy.

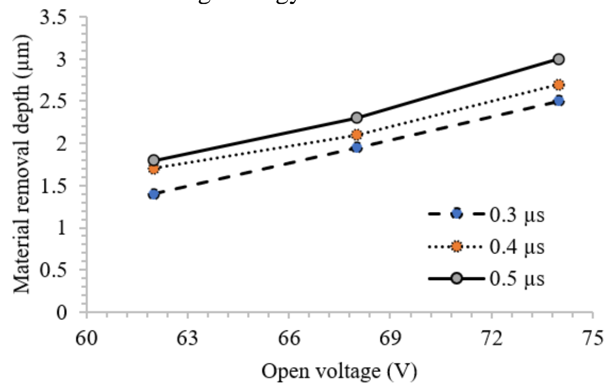

Fig. 8 Variation in material removal depth with OV at different pulse on-time

The cumulative outcome showcases a slight degree of variation. It is evident from the findings that both T_{on} and OV exert a substantial impact on material removal depth, with their influences observed to fluctuate based on the presence of the other parameter. The highest material removal depth is achieved when both T_{on} and OV are set to their maximum values.

4. Conclusions

This study introduces a transient finite element model of the wire-EDM process focused on a single discharge. The objective is to predict the workpiece's temperature and consequent material removal depth across varied process parameters. Notably, as the open voltage and pulse escalate over time, the material removal depth experiences an augmentation. The simulation outcomes also reveal that the material is heated to elevated temperatures, nearing the liquid-vapour critical point. Moreover, the observed pattern in material removal depth appears consistent across the parameters. Furthermore, it is noteworthy that the pulse on time exhibits a lower influence on material removal depth, particularly at lower open voltage values. This study could minimize the requisite number of experiments for process optimization, thereby fostering an improved understanding of the material removal mechanism in wire-EDM.

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